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Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Original) A method comprising:

in response to a first signal indicating the execution of a breakpoint by a processor, suspending execution of a peripheral and saving the state of the peripheral;

continuing execution of the breakpoint by the processor in response to receiving a second signal indicating that the state of the peripheral has been saved; and

restoring the saved state of the peripheral in response to a third signal indicating that execution of the breakpoint by the processor has been completed.

2. (Original) The method of claim 1 comprising resuming normal execution of the processor in response to a signal indicating that the saved state has been restored.

3. (Original) The method of claim 1 comprising resuming normal execution of the peripheral in response to a signal indicating that the processor has resumed normal execution.

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4. (Original) The method of claim 1 comprising setting a register to control whether generation of the second signal is to be based on the state of the peripheral.

5. (Original) The method of claim 1 comprising setting a register to control whether generation of a signal indicating that the saved state has been restored is to be based on the state of the peripheral.

6. (Previously Presented) The method of claim 1 comprising triggering the breakpoint in response to an occurrence of a condition associated with an instruction being executed by the processor.

7. (Original) A system comprising:
a processor;
a first computer-readable medium storing instructions that, when applied to the processor, cause the processor to:
generate a first signal indicating execution of a breakpoint,
continue execution of the breakpoint in response to receiving a second signal, and
generate a third signal indicating that execution of the breakpoint has been completed;
a peripheral coupled to the processor;

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a second computer-readable medium storing instructions that, when applied to the peripheral, cause the peripheral to:

- suspend execution and save a state of the peripheral, in response to receiving the first signal,
- restore the state of the peripheral, in response to receiving the third signal; and

a digital logic circuit to generate the second signal indicating that the state of the peripheral has been saved, the digital logic circuit coupled to the processor and the peripheral.

8. (Original) The system of claim 7 wherein the first computer-readable medium includes instructions that cause the processor to:

- resume normal execution in response to receiving a fourth signal, and

- generate a fifth signal indicating that the processor has resumed normal execution; and

- wherein the second computer-readable medium includes instructions that cause the peripheral to resume normal execution, in response to receiving the fifth signal; and

- wherein the digital logic circuit is configured to generate the fourth signal indicating that the saved state of the peripheral has been restored.

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9. (Original) The system of claim 8, further comprising:
a second processor;
a third computer-readable medium storing instructions that,
when applied to the second processor, cause the second processor
to:

suspend execution and save a state of the second
processor, in response to receiving the first signal,
restore the state of the second processor, in response
to receiving the third signal, and
resume normal execution, in response to receiving the
fifth signal; and

the digital logic circuit configured to:

generate the second signal indicating that the state
of the second processor has been saved, and

generate the fourth signal indicating that the saved
state of the second processor has been restored.

10. (Original) The system of claim 7 including a system
on a chip (SOC).

11. (Original) The system of claim 7 including a
debugging tool coupled to the system to debug the system.

12. (Original) The system of claim 7 wherein the digital
logic circuit comprises a register to control whether generation

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of the second signal is to be based on the state of the peripheral.

13. (Original) The system of claim 7 wherein the state identifies a state of internal registers associated with the peripheral.

14. (Original) The system of claim 7 wherein the processor operates at a clock rate different than the peripheral.

15. (Original) An apparatus comprising:
a processor having a computer-readable medium storing instructions that, when applied to the processor, cause the processor to:

generate a signal indicating execution of a breakpoint,

continue execution of the breakpoint in response to receiving a signal indicating that the state of a peripheral has been saved, and

generate a signal indicating that execution of the breakpoint has been completed.

16. (Original) The apparatus of claim 15 wherein the computer-readable medium includes instructions that cause the

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processor to resume normal execution in response to a signal indicating that the saved state has been restored.

17. (Original) An article comprising a computer-readable medium that stores computer-executable instructions for causing a computer system to:

generate a signal indicating execution of a breakpoint;

continue execution of the breakpoint in response to receiving a signal indicating that the state of a peripheral has been saved; and

generate a signal indicating that execution of the breakpoint has been completed.

18. (Original) The article of claim 17 wherein the computer-readable medium stores computer-executable instructions for causing a computer system to resume normal execution of the processor in response to a signal indicating that the saved state has been restored.

19. (Original) An apparatus comprising:

a peripheral having a computer-readable medium storing instructions that, when applied to the peripheral, cause the peripheral to:

suspend execution and save a state of the peripheral, in response to receiving a signal indicating execution of a

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breakpoint, and

restore the state of the peripheral, in response to receiving a signal indicating that execution of the breakpoint has been completed.

20. (Original) The apparatus of claim 19 wherein the computer-readable medium includes instructions that cause the peripheral to resume normal execution of the peripheral in response to a signal indicating that a processor has resumed normal execution.

21. (Original) An article comprising a computer-readable medium that stores computer-executable instructions for causing a computer system to:

suspend execution and save a state of the peripheral, in response to receiving a signal indicating execution of a breakpoint, and

restore the state of the peripheral, in response to receiving a signal indicating that execution of the breakpoint has been completed.

22. (Original) The article of claim 21 wherein the computer-readable medium stores computer-executable instructions for causing a computer system to resume normal execution of the

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peripheral in response to a signal indicating that a processor has resumed normal execution.

23. (Original) An apparatus comprising:
one or more signal lines used to receive signals and to send signals; and
a processor configured to:
generate a signal indicating execution of a breakpoint,
continue execution of the breakpoint in response to receiving a signal on a signal line indicating that the state of a peripheral has been saved, and
generate a signal on a signal line indicating that execution of the breakpoint has been completed.

24. (Original) The apparatus of claim 23 wherein the processor is configured to resume normal execution in response to a signal indicating that the saved state has been restored.

25. (Original) An apparatus comprising:
one or more signal lines used to receive signals and to send signals; and
a peripheral configured to:
suspend execution and save a state of the peripheral, in response to receiving a signal indicating execution of a

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breakpoint, and

restore the state of the peripheral, in response to receiving a signal indicating that execution of the breakpoint has been completed.

26. (Original) The apparatus of claim 25 wherein the peripheral is configured to resume normal execution in response to a signal indicating that a processor has resumed normal execution.

27. (Previously Presented) The method of claim 1 wherein saving the state of the peripheral comprises saving the state of an input/output device.

28. (Previously Presented) The method of claim 27 wherein saving the state of the input/output device comprises saving the state of a universal asynchronous receiver/transmitter (UART).

29. (Previously Presented) The method of claim 1 wherein suspending execution of the peripheral comprises suspending execution of a peripheral that is monolithically fabricated on a same chip as the processor.

30. (Previously Presented) The system of claim 7 wherein the peripheral comprises an input/output device.

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31. (Previously Presented) The system of claim 30 wherein the input/output device comprises a universal asynchronous receiver/transmitter (UART).

32. (Previously Presented) The system of claim 7 wherein the system comprises a monolithically fabricated chip that includes the processor and the peripheral.

33. (Previously Presented) The apparatus of claim 15 wherein the computer-readable medium includes instructions that cause the processor to continue execution of the breakpoint in response to receiving a signal indicating that the state of an input/output device has been saved.

34. (Previously Presented) The apparatus of claim 33 wherein the computer-readable medium includes instructions that cause the processor to continue execution of the breakpoint in response to receiving a signal indicating that the state of a universal asynchronous receiver/transmitter (UART) has been saved.

35. (Previously Presented) The apparatus of claim 15 wherein the apparatus comprises a monolithically fabricated chip that includes the processor and the peripheral.

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36. (Previously Presented) The article of claim 17 wherein the computer-readable medium stores computer-executable instructions for causing a computer system to continue execution of the breakpoint in response to receiving a signal indicating that the state of an input/output device has been saved.

37. (Previously Presented) The article of claim 36 wherein the computer-readable medium stores computer-executable instructions for causing a computer system to continue execution of the breakpoint in response to receiving a signal indicating that the state of a universal asynchronous receiver/transmitter (UART) has been saved.

38. (Previously Presented) The apparatus of claim 20 wherein the apparatus comprises a monolithically fabricated chip that includes the processor and the peripheral.

39. (Previously Presented) The apparatus of claim 23 wherein the apparatus comprises a monolithically fabricated chip that includes the processor and the peripheral.

40. (Previously Presented) The system of claim 25 wherein the peripheral comprises an input/output device.

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41. (Previously Presented) The system of claim 40 wherein the input/output device comprises a universal asynchronous receiver/transmitter (UART).

42. (Previously Presented) The apparatus of claim 26 wherein the apparatus comprises a monolithically fabricated chip that includes the processor and the peripheral.